1. (Previously Submitted) A system for processing digital signals comprising symbols propagated according to a period, the system comprising:

a signal conditioning filter comprising a first stage for mitigating degradations of a digital signal that occur according to a first time scale, the first stage comprising a linear tapped-delay line filter tuned to the first time scale, the first time scale comprising a fraction of the period at which the symbols are propagated, and a second stage for removing signal distortions that occur according to a second time scale, the second stage comprising a linear tapped-delay line filter tuned to the second time scale, the second time scale being different than the first time scale and comprising a magnitude at least equal to the period at which the symbols are propagated; and

a signal integrity unit for controlling the signal conditioning filter by maximizing fidelity of the digital signals.

2. (Cancelled.)

3. (Previously Submitted) The system of Claim 1, wherein the signal conditioning filter comprises a coefficient amplifier, the coefficient amplifier comprising a Gilbert cell multiplier.

4. (Previously Submitted) The system of Claim 1, wherein each tapped delay-line filter comprises LC circuits.

5. (Previously Submitted) The system of Claim 1, wherein delays are distributed across both input and output branches of each tapped delay-line filter.

6. (Previously Submitted) The system of Claim 1, wherein parasitic capacitances from one of an input and output of each tapped-delay line filter are absorbed into an LC design circuit and are used to implement the delay.

7. (Original) The system of Claim 1, wherein the digital signals comprise binary signals.

8. (Original) The system of Claim 1, wherein the digital signals comprise multilevel signals.

9. (Previously Submitted) The system of Claim 1, wherein the first and second stages comprise various signal paths of different lengths where time delays produced by the signal paths are re-used.

10. (Previously Submitted) A system for processing digital signals comprising:

a first filter stage comprising a first linear tapped-delay line filter tuned to a first time constant, the first time constant comprising a value that is less than a symbol period, for compensating for signal distortions that occur within a single symbol period and for integrating over less than a symbol period in order to substantially reduce at least one of ringing, jitter, and noise; and

a second filter stage comprising a second linear tapped-delay line filter tuned to a second time constant, the first time constant being smaller than the second time constant and the second time constant comprising value at least equal to a symbol period, the second filter stage for removing inter-symbol interference (ISI).

11. (Cancelled).

12. (Previously Submitted) The system of Claim 10, wherein each filter comprises a coefficient amplifier, the coefficient amplifier comprising a Gilbert cell multiplier.

13. (Previously Submitted) The system of Claim 10, wherein each tapped delay-line filter comprises LC circuits.

14. (Previously Submitted) The system of Claim 10, wherein delays are distributed across both input and output branches of each tapped delay-line filter.

15. (Previously Submitted) The system of Claim 10, wherein parasitic capacitances from one of an input and output of each tapped-delay line filter are absorbed into the LC design circuit and are used to implement the delay.

16. (Previously Submitted) The system of Claim 10, wherein the digital signals comprise binary signals.

17. (Previously Submitted) The system of Claim 10, wherein the digital signals comprise multilevel signals.

18. (Previously Submitted) The system of Claim 10, wherein the first and second filtering stages form part of a unit for receiving digital signals.

19. (Previously Submitted) The system of Claim 10, wherein the first and second filtering stages form part of a unit for transmitting digital signals.

20. (Previously Submitted) A system for processing digital signals comprising symbols propagated according to a period, the system comprising:

a cascade of two linear filters, where each filter comprises a series of variable gain amplifiers connected by delay elements, each delay element for a respective filter having a same delay value, each linear filter equalizing a particular frequency band of a multilevel signal;

the delay elements in the first filter being tuned to a fraction of the symbol period at which the symbols are propagated for compensating for signal distortions that occur within a single symbol period and for integrating over less than a symbol period in order to substantially reduce at least one of ringing, jitter, and noise;

the delay elements in the second filter being tuned to a magnitude at least equal to the symbol period at which symbols are propagated for mitigating degradations that occur according to the period.

21. (Previously Submitted) The system of Claim 20, wherein each variable gain amplifier comprises a Gilbert Cell multiplier.

22. (Previously Submitted) The system of Claim 20, wherein the delay elements of the first and second filters comprise delay lines.

23. (Previously Submitted) The system of Claim 20, wherein the delay elements of the first and second filters comprise delay lines that include LC circuits.

24. (Original) The system of Claim 20, further comprising a signal integrity unit for controlling each filter.

25. (Previously Submitted) The system of Claim 24, wherein the signal integrity unit measures fidelity of a filtered signal, each filter further comprising a variable gain coefficient amplifier, and gains of each variable gain coefficient amplifier are controlled to maximize fidelity measured by the signal integrity unit.

26-35. (Cancelled).

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